We claim:

1. A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NAND gate having an internal circuit node, a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NAND gate having an internal circuit node, a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit coupled between the internal node of the first NAND gate and the internal node of the second NAND gate.

2. The SR flip-flop of claim 1 in which the first NAND gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a voltage source, and a drain coupled to the output;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the voltage source, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to the internal circuit node; and

a second N-channel transistor having a drain coupled to the internal circuit node, a gate coupled to the first input, and a source coupled to ground.

3. The SR flip-flop of claim 1 in which the first NAND gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a first controlled power supply, and a drain coupled to the output;

a second P-channel transistor having a gate coupled to the second

input, a source coupled to the first controlled power supply, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to the internal circuit node; and

a second N-channel transistor having a drain coupled to the internal circuit node, a gate coupled to the first input, and a source coupled to a second controlled power supply.

4. The SR flip-flop of claim 1 in which the second NAND gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a voltage source, and a drain coupled to the output;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the voltage source, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to the internal circuit node; and

a second N-channel transistor having a drain coupled to the internal circuit node, a gate coupled to the first input, and a source coupled to ground.

5. The SR flip-flop of claim 1 in which the second NAND gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a first controlled power supply, and a drain coupled to the output;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the first controlled power supply, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to the internal circuit node; and

a second N-channel transistor having a drain coupled to the internal

circuit node, a gate coupled to the first input, and a source coupled to a second controlled power supply.

6. The SR flip-flop of claim 1 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the internal circuit node of the first NAND gate and ground;

a second ferroelectric capacitor coupled between the internal circuit node of the second NAND gate and ground; and

a third ferroelectric capacitor coupled between the internal circuit nodes of the first and second NAND gates.

7. The SR flip-flop of claim 1 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the internal circuit node of the first NAND gate and ground;

a second ferroelectric capacitor coupled between the internal circuit node of the second NAND gate and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the internal circuit nodes of the first and second NAND gates.

8. The SR flip-flop of claim 1 further comprising means for selectively coupling the ferroelectric capacitor circuit to the internal nodes of the first and second NAND gates.

9. The SR flip-flop of claim 1 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the internal nodes of the first and second NAND gates.

10. The SR flip-flop of claim 1 further comprising a precharge circuit coupled to the first and second NAND gates.

11. The SR flip-flop of claim 1 further comprising an equalization circuit coupled to the first and second NAND gates.

12. The SR flip-flop of claim 1 further comprising a gate control circuit coupled to the first and second NAND gates.

13. The SR flip-flop of claim 1 in which the first and second NAND gates further comprise an internal drive isolation circuit.

14. A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NOR gate having an internal circuit node, a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NOR gate having an internal circuit node, a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit coupled between the internal node of the first NOR gate and the internal node of the second NOR gate.

15. The SR flip-flop of claim 1 in which the first NOR gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a voltage source, and a drain coupled to the internal node;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the internal node, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the first input, and a source coupled to ground; and

a second N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to ground.

16. The SR flip-flop of claim 1 in which the first NOR gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a first controlled power supply, and a drain coupled to the internal circuit node;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the internal circuit node, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the first input, and a source coupled to a second controlled power supply; and

a second N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to the second controlled power supply.

17. The SR flip-flop of claim 1 in which the second NOR gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a voltage source, and a drain coupled to the internal circuit node;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the internal circuit node, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the first input, and a source coupled to ground; and

a second N-channel transistor having a drain coupled to the output, a gate coupled to the second input, and a source coupled to ground.

18. The SR flip-flop of claim 1 in which the second NOR gate comprises:

a first P-channel transistor having a gate coupled to the first input, a source coupled to a first controlled power supply, and a drain coupled to the internal circuit node;

a second P-channel transistor having a gate coupled to the second input, a source coupled to the internal circuit node, and a drain coupled to the output;

a first N-channel transistor having a drain coupled to the output, a gate coupled to the first input, and a source coupled to a second controlled power supply; and

a second N-channel transistor having a drain coupled to the output, a

gate coupled to the second input, and a source coupled to the second controlled power supply.

19. The SR flip-flop of claim 1 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the second input of the first NOR gate and ground;

a second ferroelectric capacitor coupled between the second input of the second NOR gate and ground; and

a third ferroelectric capacitor coupled between the second inputs of the first and second NOR gates.

20. The SR flip-flop of claim 1 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the second input of the first NOR gate and ground;

a second ferroelectric capacitor coupled between the second input of the second NOR gate and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the second inputs of the first and second NOR gates.

21. The SR flip-flop of claim 1 further comprising means for selectively coupling the ferroelectric capacitor circuit to the second inputs of the first and second NOR gates.

22. The SR flip-flop of claim 1 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the second inputs of the first and second NOR gates.

23. The SR flip-flop of claim 1 further comprising a precharge circuit coupled to the first and second NOR gates.

24. The SR flip-flop of claim 1 further comprising an equalization circuit coupled to the first and second NOR gates.

25. The SR flip-flop of claim 1 further comprising a gate control circuit coupled to the first and second NOR gates.

26. The SR flip-flop of claim 1 in which the first and second NOR gates further comprise an internal drive isolation circuit.

27. A ferroelectric, non-volatile, JK flip-flop comprising:

a J input;

a K input;

a Q output;

a complementary Q output;

a ferroelectric, non-volatile SR flip-flop including a set input, a reset input, a Q output coupled to the Q output of the JK flip-flop, and a complementary Q output coupled to the complementary Q output of the JK flip-flop;

a first NAND gate having a first input coupled to the Q output of the JK flip-flop, a second input coupled to the K input, a third input for receiving a clock signal and an output coupled to the set input;

a second NAND gate having a first input for receiving the clock signal, a second input coupled to the J input, a third input coupled to the complementary Q output of the JK flip-flop.

28. The JK flip-flop of claim 27 in which the SR flip-flop comprises a NAND-gate based flip-flop.

29. The JK flip-flop of claim 27 in which the SR flip-flop comprising a NOR-gate based flip-flop.

30. The JK flip-flop of claim 27 further comprising a first controlled power supply coupled to the SR flip-flop.

31. The JK flip-flop of claim 30 further comprising a second controlled power supply coupled to the SR flip-flop.

32. The JK flip-flop of claim 27 in which the SR flip-flop comprises a

ferroelectric capacitor circuit including first, second, and third ferroelectric capacitors.

33. The JK flip-flop of claim 32 in which one of the ferroelectric capacitors comprises two serially-coupled matched ferroelectric capacitors.

34. The JK flip-flop of claim 32 further comprising means for selectively coupling the ferroelectric capacitor circuit.

35. The JK flip-flop of claim 27 further comprising a precharge circuit coupled to the SR flip-flop.

36. The JK flip-flop of claim 27 further comprising an equalization circuit coupled to the SR flip-flop.

37. The JK flip-flop of claim 27 further comprising a gate control circuit coupled to the SR flip-flop.

38. The JK flip-flop of claim 27 in which the SR flip-flop further comprises an internal drive isolation circuit.

39. A ferroelectric, non-volatile, master-slave JK flip-flop comprising:

a J input;

a K input;

a Q output;

a complementary Q output;

a clock input;

a complementary clock input;

a ferroelectric, non-volatile master JK flip-flop for receiving the J, K, and clock inputs, and having a Q output and a complementary Q output;

a slave JK flip-flop coupled to the complementary clock input, and the Q and complementary Q outputs of the master JK flip-flop, and having a Q output coupled to the Q output of the master-slave JK flip-flop and a complementary Q output coupled to the complementary Q output of the master-slave JK flip-flop.

40. The master-slave flip-flop of claim 39 in which the master flip-flop

comprises a NAND-gate based flip-flop.

41. The master-slave flip-flop of claim 39 in which the master flip-flop comprises a NOR-gate based flip-flop.

42. The master-slave flip-flop of claim 39 in which the slave flip-flop comprises a NAND-gate based flip-flop.

43. The master-slave flip-flop of claim 39 in which the slave flip-flop comprises a NOR-gate based flip-flop.

44. The master-slave flip-flop of claim 39 further comprising at least one controlled power supply coupled to the master flip-flop.

45. The master-slave flip-flop of claim 39 further comprising at least one controlled power supply coupled to the slave flip-flop.

46. The master-slave flip-flop of claim 39 in which the master flip-flop comprises a ferroelectric capacitor circuit including first, second, and third ferroelectric capacitors.

47. The master-slave flip-flop of claim 46 in which one of the ferroelectric capacitors comprises two serially-coupled matched ferroelectric capacitors.

48. The master-slave flip-flop of claim 46 further comprising means for selectively coupling the ferroelectric capacitor circuit.

49. The master-slave flip-flop of claim 39 in which the slave flip-flop comprises a non-volatile ferroelectric flip-flop.

50. The master-slave flip-flop of claim 39 in which the slave flip-flop comprises a ferroelectric capacitor circuit including first, second, and third ferroelectric capacitors.

51. The master-slave flip-flop of claim 50 in which one of the ferroelectric capacitors comprises two serially-coupled matched ferroelectric

capacitors.

52. The master-slave flip-flop of claim 50 further comprising means for selectively coupling the ferroelectric capacitor circuit.

53. The master-slave flip-flop of claim 39 further comprising a precharge circuit coupled to the master flip-flop.

54. The master-slave flip-flop of claim 39 further comprising a precharge circuit coupled to the slave flip-flop.

55. The master-slave flip-flop of claim 39 further comprising an equalization circuit coupled to the master flip-flop.

56. The master-slave flip-flop of claim 39 further comprising an equalization circuit coupled to the slave flip-flop.

57. The JK flip-flop of claim 39 further comprising a gate control circuit coupled to the master flip-flop.

58. The JK flip-flop of claim 39 further comprising a gate control circuit coupled to the slave flip-flop.

59. The JK flip-flop of claim 39 in which the master flip-flop further comprises an internal drive isolation circuit.

60. The JK flip-flop of claim 39 in which the slave flip-flop further comprises an internal drive isolation circuit.

61. A ferroelectric, non-volatile, D-type flip-flop comprising:

a D input;

a Q output;

a clocked transmission-gate based master stage having an inputs coupled to the D input, and an output;

a ferroelectric, non-volatile, transmission-gate based slave stage having an input coupled to the output of the master stage, and an output coupled to the Q output.

62. The D-type flip-flop of claim 61 in which the slave stage comprises:

a first clocked transmission gate having an input forming the input of the slave stage and an output;

a first controlled inverter having an input coupled to the output of the first clocked transmission gate, and an output;

a first non-clocked transmission gate having an input coupled to the output of the first controlled inverter and an output coupled to the output of the slave stage;

a second clocked transmission gate having an input, and an output coupled to the output of the first clock transmission gate;

a second controlled inverter having an input coupled to the output of the slave stage, and an output coupled to the input of the second clocked transmission gate;

a second non-clocked transmission gate having an input coupled to the output of the slave stage and an output coupled to ground; and

a ferroelectric capacitor circuit coupled between the output of the first clocked transmission gate and the output of the slave stage.

63. The D-type flip-flop of claim 62 in which the ferroelectric capacitor circuit comprises first, second, and third ferroelectric capacitors.

64. The D-type flip-flop of claim 63 in which one of the ferroelectric capacitors comprises two serially-coupled matched ferroelectric capacitors.

65. The D-type flip-flop of claim 62 further comprising means for selectively coupling the ferroelectric capacitor circuit.

66. The D-type flip-flop of claim 61 further comprising a precharge circuit coupled to the slave stage.

67. The D-type flip-flop of claim 61 further comprising an equalization circuit coupled to the slave stage.

68. The D-type flip-flop of claim 61 further comprising asychronous set and clear inputs.

69. A ferroelectric, non-volatile, D-type flip-flop comprising:

a D input;

a Q output;

a ferroelectric, non-volatile, transmission-gate based master stage having an input coupled to the D input, and an output.

a clocked transmission-gate based slave stage having an input coupled to the output of the master stage, and an output coupled to the Q output;

70. The D-type flip-flop of claim 69 in which the master stage comprises:

a first clocked transmission gate having an input forming the input of the master stage and an output;

a first controlled inverter having an input coupled to the output of the first clocked transmission gate, and an output;

a first non-clocked transmission gate having an input coupled to the output of the first controlled inverter and an output coupled to the output of the master stage;

a second clocked transmission gate having an input, and an output coupled to the output of the first clocked transmission gate;

a second controlled inverter having an input coupled to the output of the master stage, and an output coupled to the input of the second clocked transmission gate; and

a ferroelectric capacitor circuit coupled between the output of the first clocked transmission gate and the output of the master stage.

71. The D-type flip-flop of claim 70 in which the ferroelectric capacitor circuit comprises first, second, and third ferroelectric capacitors.

72. The D-type flip-flop of claim 71 in which one of the ferroelectric capacitors comprises two serially-coupled matched ferroelectric capacitors.

73. The D-type flip-flop of claim 71 further comprising means for selectively coupling the ferroelectric capacitor circuit.

74. The D-type flip-flop of claim 69 further comprising a precharge

circuit coupled to the master stage.

75. The D-type flip-flop of claim 69 further comprising an equalization circuit coupled to the master stage.

76. The D-type flip-flop of claim 69 further comprising asychronous set and clear inputs.

77. An N-bit non-volatile serial-in, serial-out shift register comprising:

N ferroelectric, non-volatile D-type flip-flops each having a D input, a Q output, a clock input, and a ferroelectric control input, wherein

the D input of a first flip-flop forms the shift register input,

the Q output of an Nth flip-flop forms the shift register output,

the Q output of an (N-1)th flip-flop is coupled to the input of an Nth flip-flop such that all of the flip-flops are serially coupled together,

the clock inputs of each of the flip-flops are coupled together and to a clock bus, and

the ferroelectric control inputs of each of the flip-flops are coupled together and to a ferroelectric control bus.

78. The shift register of claim 77 in which N is equal to eight.

79. An N-bit non-volatile parallel-in, serial-out shift register comprising:

N multiplexers each having a first input, a second input, a select input, and an output; and

N ferroelectric, non-volatile D-type flip-flops each having a D input, a Q output, a clock input, and a ferroelectric control input, wherein

the output of an Nth multiplexer being coupled to the D input of an Nth flip-flop,

the Q output of an Nth flip-flop being coupled to the first input of an (N+1)th multiplexer, such that all of the multiplexers and flip-flops are coupled together,

the clock inputs of each of the flip-flops are coupled together and to a clock bus,

the ferroelectric control inputs of each of the flip-flops are coupled together and to a ferroelectric control bus,

the second inputs of each of the multiplexers form a parallel input,

the select inputs of each of the multiplexers are coupled together and to a select bus, and

the Q output of a last flip-flop forms a serial output.

80. The shift register of claim 79 in which N is equal to four.